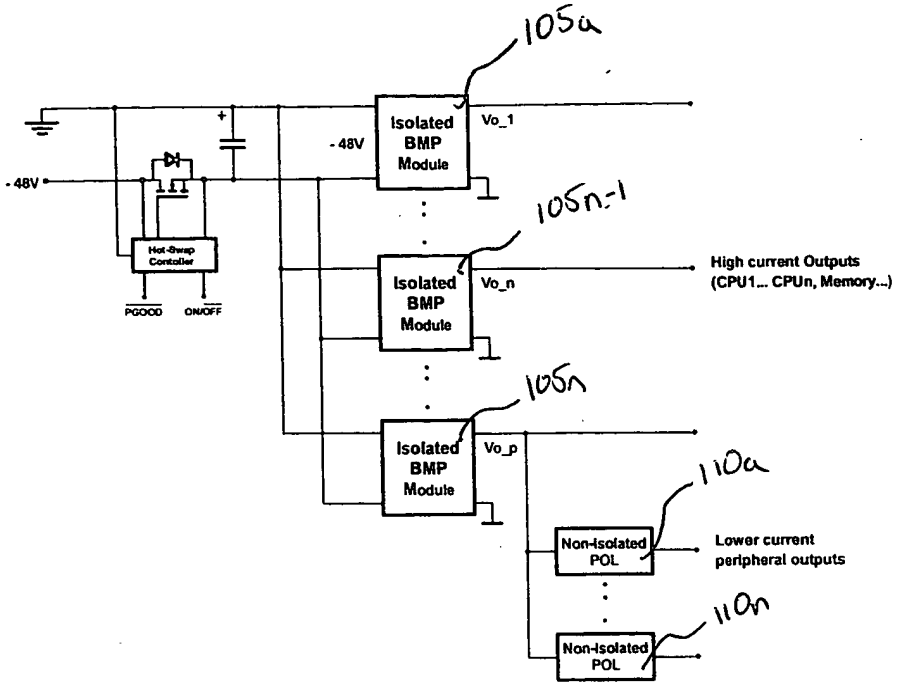


Figure 1.: Traditional on-board power distribution.

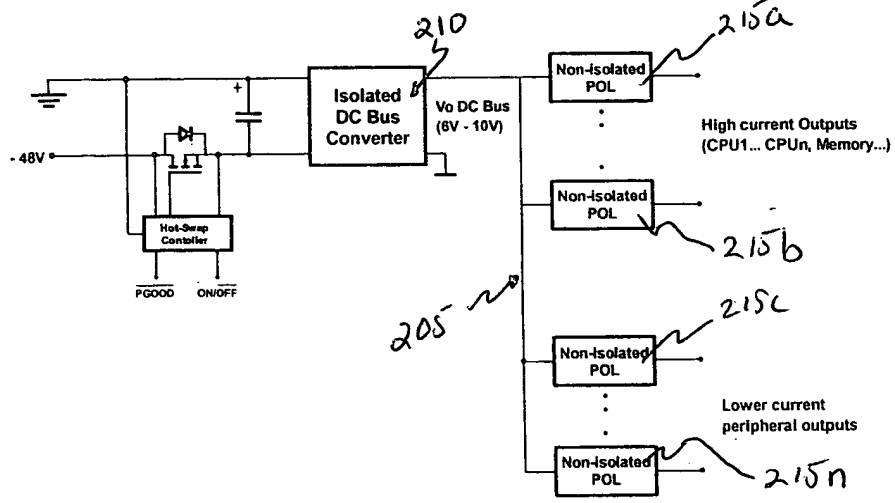


Figure 2

Optimal distributed power architecture (DPA)

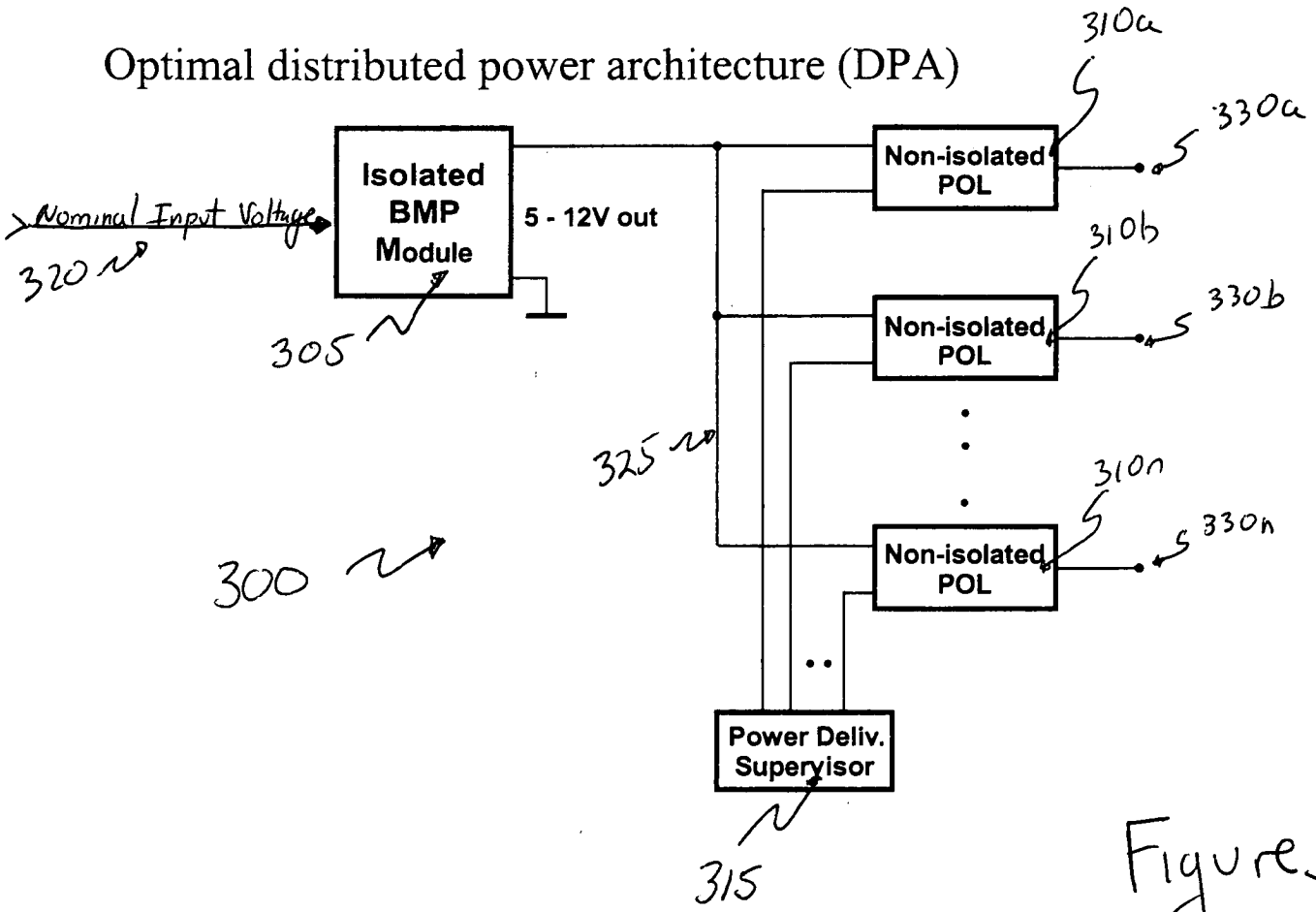


Figure3

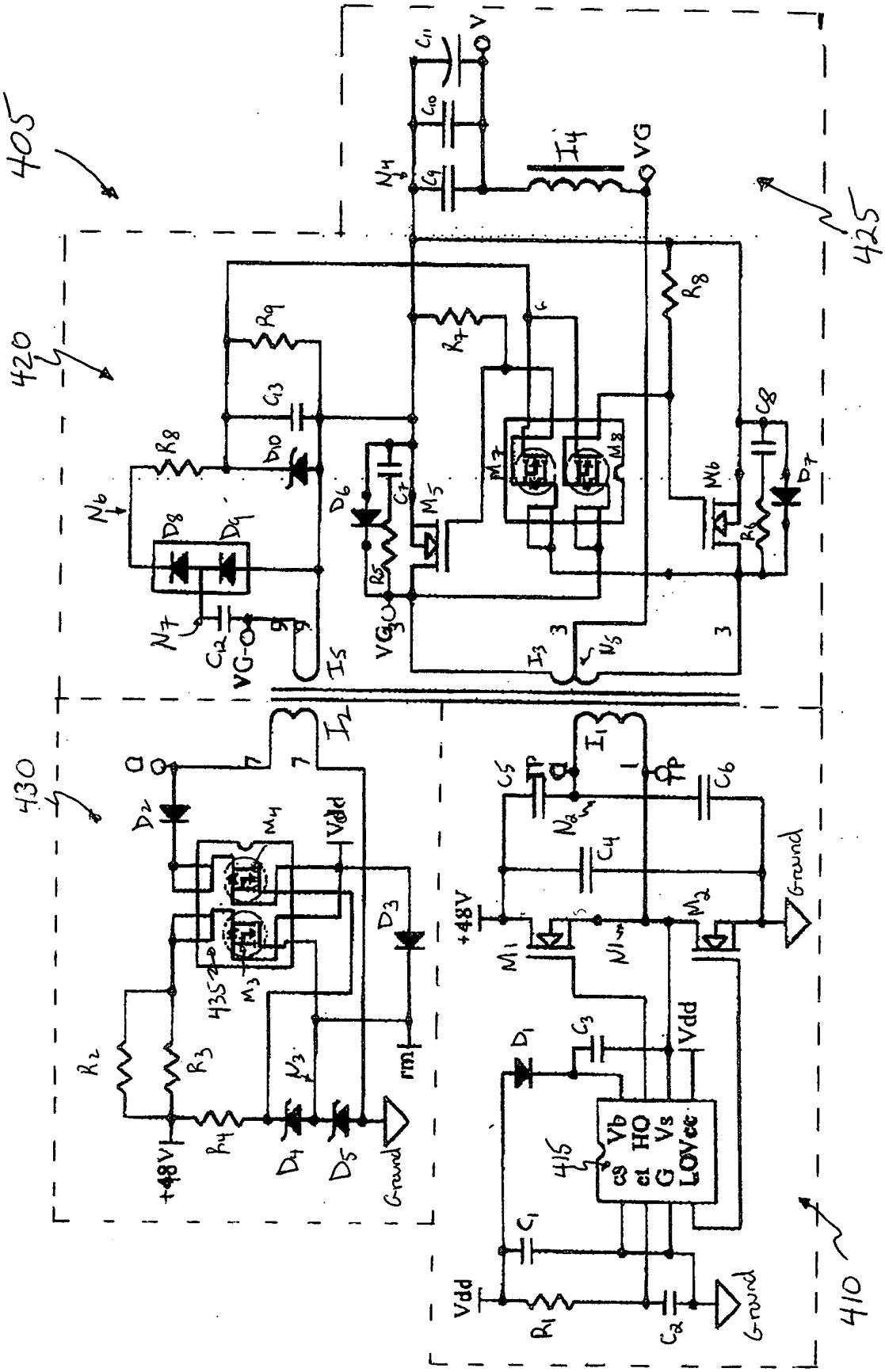


Figure 4

Figure 5

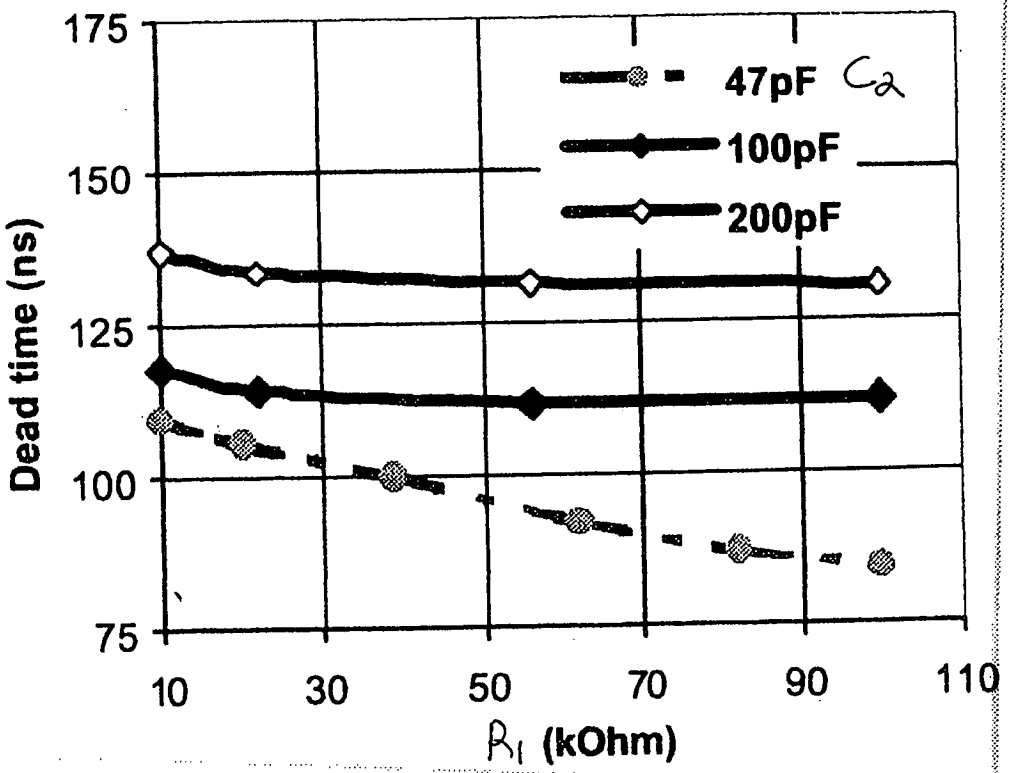
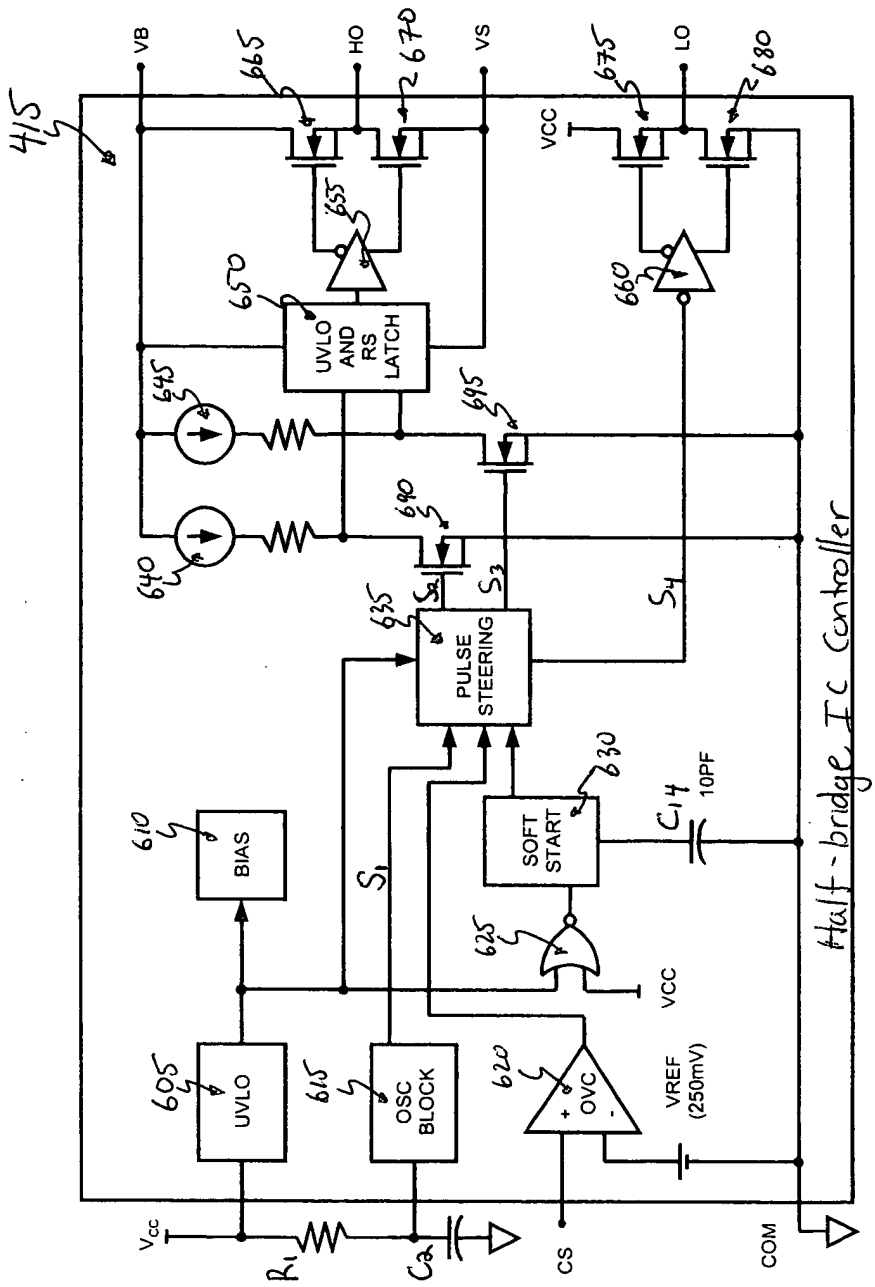

175
150
125
100
75
Dead time (ns)
47pF C_2
100pF
200pF
10
30
50
70
90
110
R_1 (kOhm)

Figure 6


415
VB
665
HO
670
VS
675
LO
680
VCC
655
660
650
UVLO AND RS LATCH
645
695
690
640
S2
S3
S4
635
PULSE STEERING
610
BIAS
S1
630
SOFT START
C14
10PF
625
VCC
605
UVLO
615
OSC BLOCK
620
OVC
VREF (250mV)
Half-bridge IC Controller
Vcc
R1
Ca
CS
COM

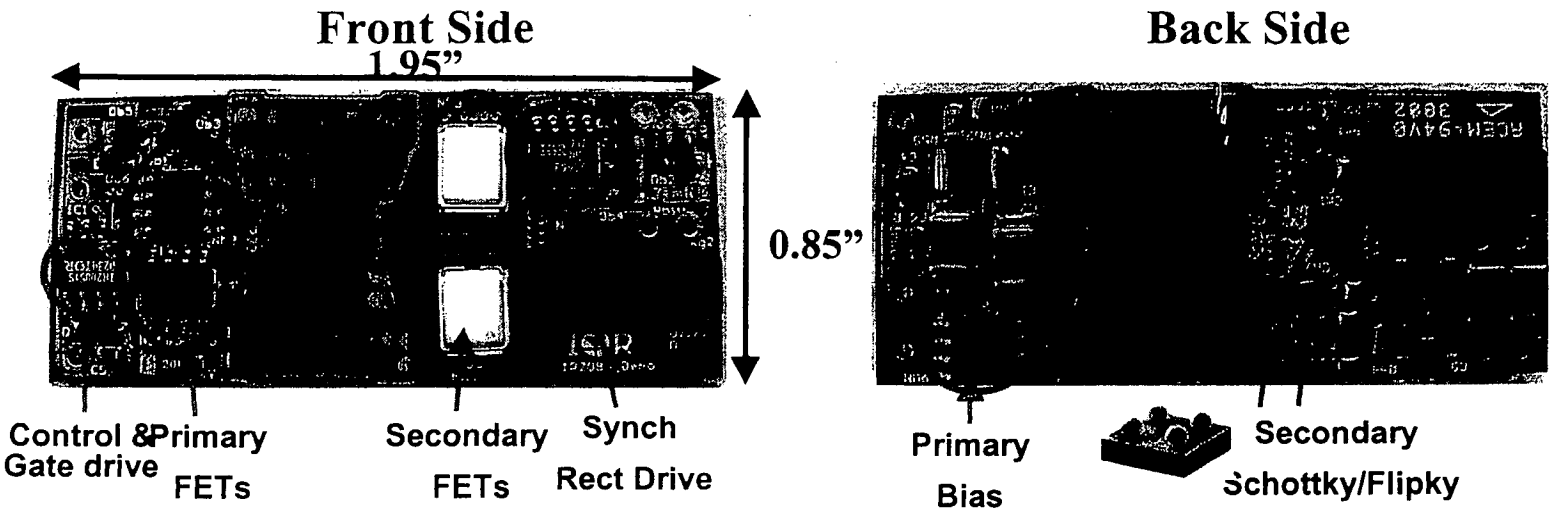
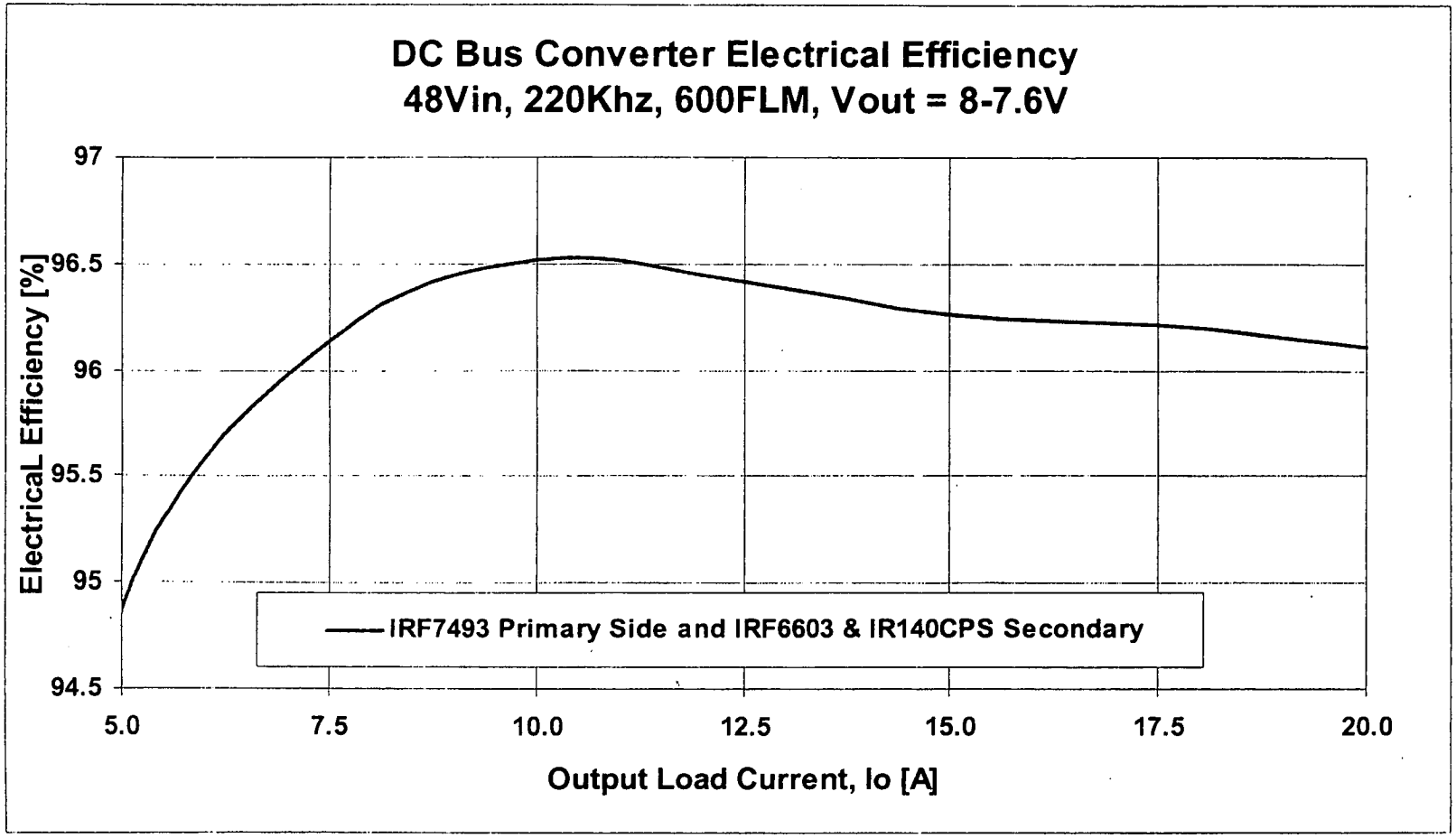

Front Side
1.95"
0.85"
Back Side
Control &
Gate drive
Primary
FETs
Secondary
FETs
Synch
Rect Drive
Primary
Bias
Secondary
Schottky/Flipky

Figure 7

Figure 8


DC Bus Converter Electrical Efficiency
48Vin, 220Khz, 600FLM, Vout = 8-7.6V
97
96.5
96
95.5
95
94.5
ElectricaL Efficiency [%]
IRF7493 Primary Side and IRF6603 & IR140CPS Secondary
5.0
7.5
10.0
12.5
15.0
17.5
20.0
Output Load Current, Io [A]

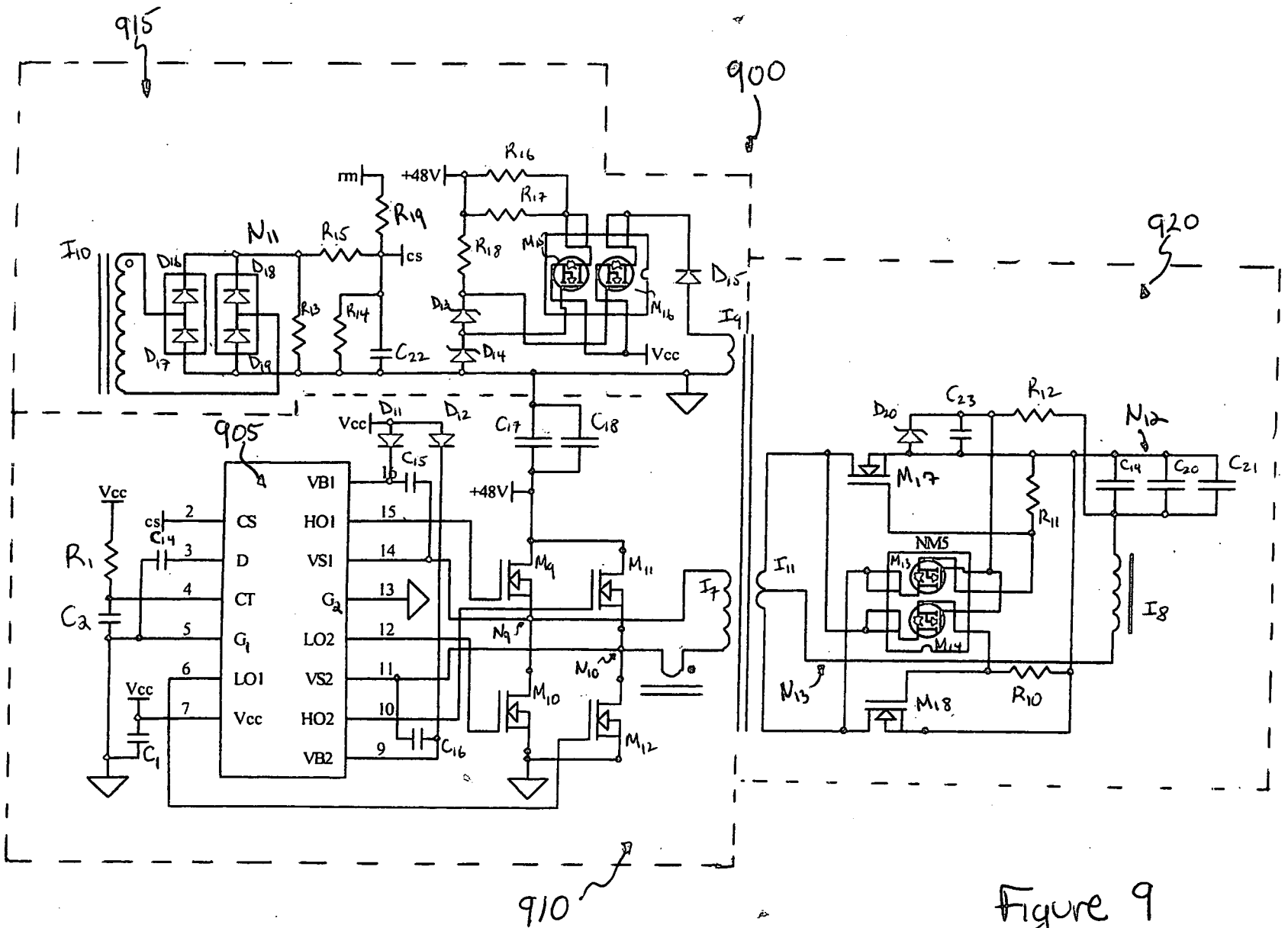

915
900
920
905
910
+48V
Vcc
cs
N11
N12
N13
R19
R15
R16
R17
R18
R13
R14
R12
R11
R10
C22
C23
C14
C20
C21
C15
C16
C17
C18
C1
C2
D16
D17
D18
D19
D20
D11
D12
D13
D14
D15
M9
M10
M11
M12
M13
M14
M16
M17
M18
NMS
I10
I11
I7
I8
I9
CS
D
CT
G1
LO1
Vcc
VB1
HO1
VS1
G2
LO2
VS2
HO2
VB2

Figure 9

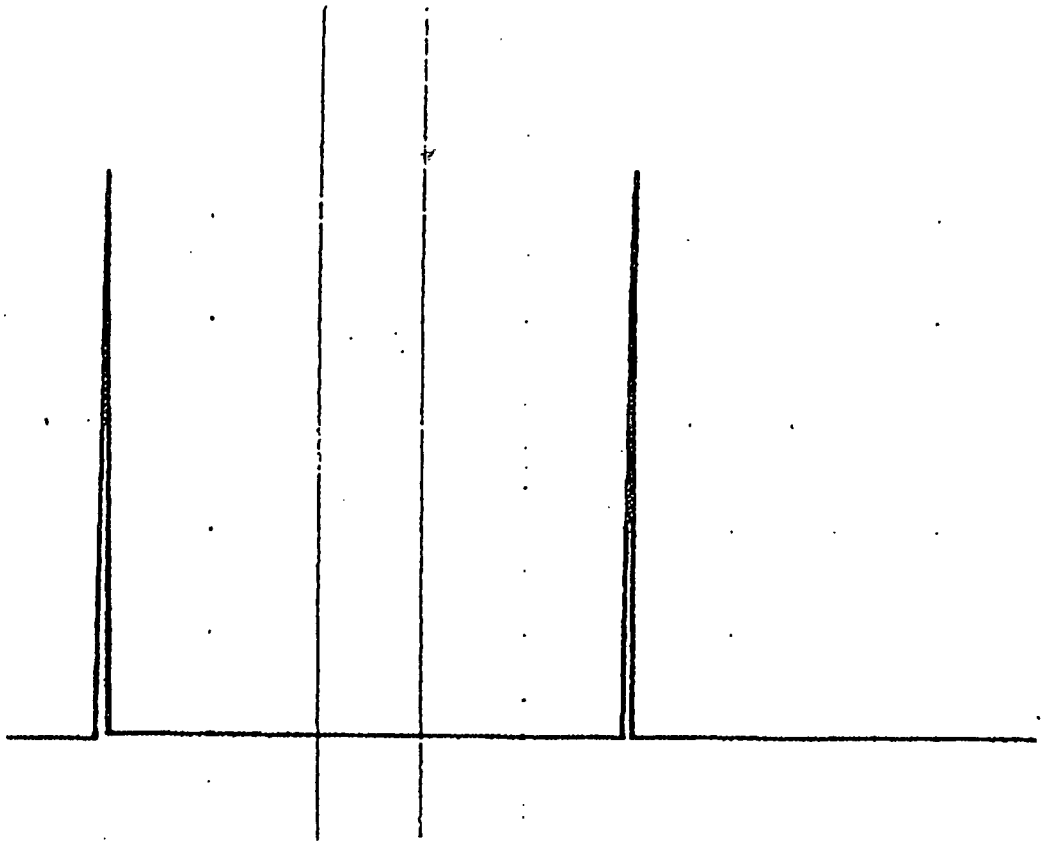
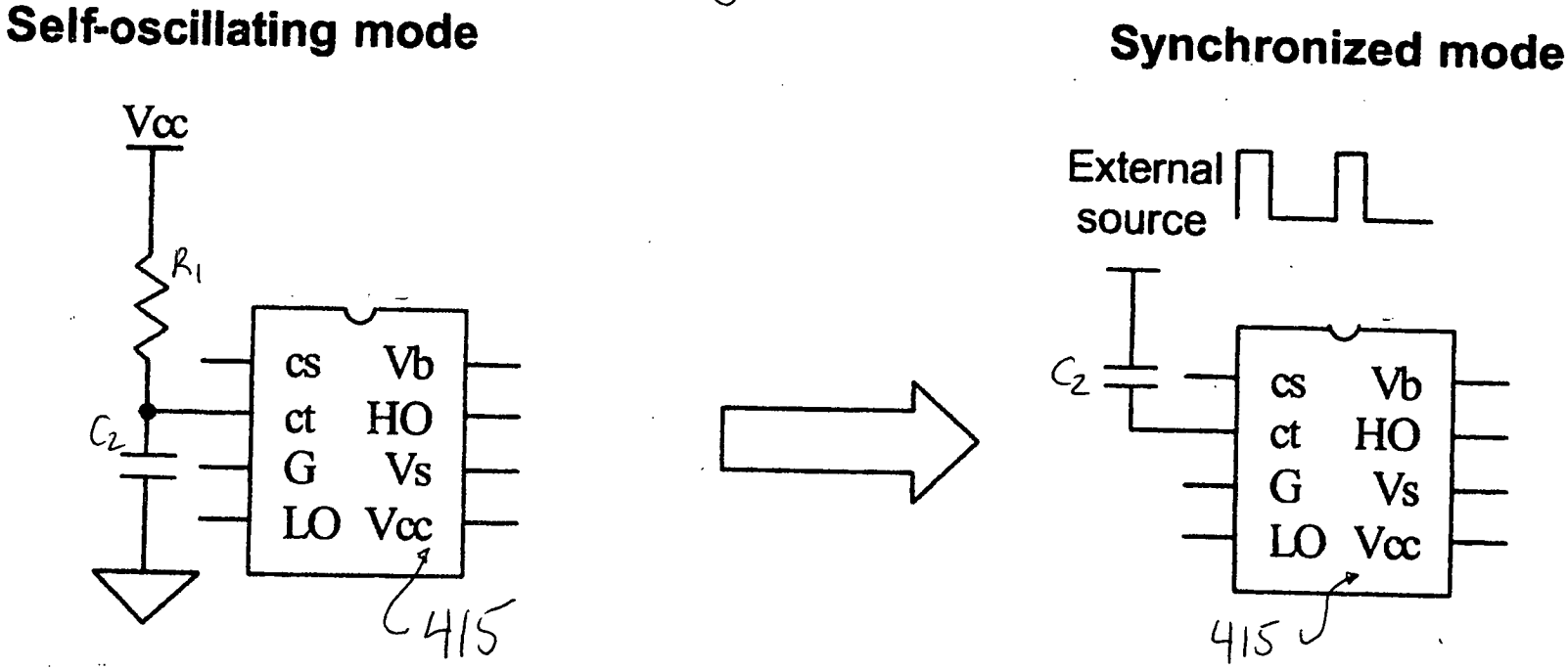


Fig. 10: Output voltage waveform during hiccup mode at current limit setting of 21A, current load setting 22A and input voltage 48V

Figure 11


Self-oscillating mode
Vcc
R1
C2
cs
ct
G
LO
Vb
HO
Vs
Vcc
415
Synchronized mode
External source
C2
cs
ct
G
LO
Vb
HO
Vs
Vcc
415